UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/631,198 | 08/03/2000 | Michael A. Lamson | TI-28674 | 9326 |

7590 03/11/2004

Gary C Honeycutt
Texas Instruments Incorporated
MS 3999
P O Box 655474
Dallas, TX 75265

| EXAMINER | |
|---|---|
| NGUYEN, DILINH P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/631,198 | LAMSON ET AL. | |
| | Examiner | Art Unit | |
| | DiLinh Nguyen | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22 and 30-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-22* is/are allowed.

6)☒ Claim(s) *30-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 30-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Kalidas et al. (U.S. 6396136).

Kalidas et al. disclose a semiconductor device (figs. 4a-4c, column 5, lines 10 et seq.) having:

a susbtrate 420 having first and second opposing surfaces, the substrate comprising:

a plurality of signal lines 401, a plurality of first power lines 402 coupleable to a first power source (column 5, lines 46-47), and a plurality of second power lines 403 coupleable to a second power source (column 6, lines 15-20), all on the second surface, at least one of the plurality of signal lines disposed between a pair of the plurality of first power lines, and the signal lines between the pair of the plurality of first power lines and the pair of the plurality of first power lines disposed between a pair of the second power lines (figs. 4b-4c); and

an integrated circuit chip 400 mounted on the substrate.

- Regarding claim 31, Kalidas et al. disclose the signal lines 401 are of a first width different from the first, the first power lines 402 are of a second width, and the second power lines 403 are of a third width different from the first and second widths.
- Regarding claim 32, Kalidas et al. disclose the third width is wider than the second width, and the second width is wider than the first width.
- Regarding claim 33, Kalidas et al. disclose a ground plane 404 (fig. 4a) on the first surface of the substrate.
- Regarding claim 34, Kalidas et al. disclose a substrate 420 having first and second opposing surfaces, the substrate having thereon: a plurality of group of lines, the plurality of groups of lines including groups of lines of at least three different widths disposed on the second surface of the substrate, the groups of lines arranged such that one or more lines in a first group of lines of a first width 401 are disposed between lines of a second group of lines of a second width 402, and lines in the second group of lines of the second width are disposed between lines of the third width 403; and an integrated circuit chip 400 mounted on the substrate and coupled to at least some of the lines.
- Regarding claim 35, Kalidas et al. disclose the lines of the first width are signal lines 401, the lines of the second width are power lines 402 coupled to a first voltage potential (column 5, lines 55-63), and the lines of the third width are power lines coupled to a second voltage potential (column 6, lines 15-20).

- Regarding claim 36, Kalidas et al. disclose a ground plane 404 on the first surface of the substrate.
- Regarding claim 37, Kalidas et al. disclose a packaged integrated circuit (figs. 4a-4c), comprising:

a substrate 420 having first and second opposing surfaces, the substrate having: a plurality of signal lines 401, a plurality of first power lines 402 coupled to a first power source (column 5, lines 46-47), and a plurality of second power lines 403 coupled to a second power source (column 6, lines 15-20), all on the second surface, at least one of the plurality of signal lines disposed between a pair of the plurality of first power lines, and the signal lines between the pair of the plurality of first power lines and the pair of the plurality of first power lines disposed between a pair of the second power lines (figs. 4b-4c); and

an integrated circuit chip 400 mounted on the substrate.

- Regarding claim 38, Kalidas et al. disclose the signal lines are of a first width, the first power lines are of a second width different from the first, and the second power lines are of a third width different from the first and second widths.
- Regarding claim 39, Kalidas et al. disclose the third width is wider than the second width, and the second width is wider than the first width.

3. Claim 34 is rejected under 35 U.S.C. 102(e) as being anticipated by Washida et al. (U.S. 5877548).

Washida et al. disclose a semiconductor device comprising:

a substrate 51 having first and second opposing surface (fig. 9), the substrate having: a plurality of groups of lines, the plurality of groups of lines including groups of lines of at least three different widths disposed on the second surface of the substrate, the groups of lines arranged such that one or more lines 3 in a first group of lines of a first width are disposed between lines of a second group of lines of a second width (cover fig.) and lines in the second group of lines of the second width are disposed between lines of the third width; and an chip 2/21 (cover fig. and figs. 9-10) mounted on the substrate and coupled to at least some of the lines.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 34 is rejected under 35 U.S.C. 102(b) as being anticipated by Link et al. (U.S. Pat. 5055704).

Link et al. disclose a semiconductor device comprising:

a substrate 16 having first and second opposing surface (fig. 4), the substrate having: a plurality of groups of lines, the plurality of groups of lines including groups of lines of at least three different widths disposed on the second surface of the substrate, the groups of lines arranged such that one or more lines in a first group of lines of a first width are disposed between lines of a second group of lines of a second width and lines in the second group of lines of the second width are disposed between lines of the third

width; and an chip 132 mounted on the substrate and coupled to at least some of the lines.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 30-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi (U.S. Pat. 5497030) in view of Tsubosaki et al. (U.S. Pat. 6137159).

- Regarding claims 30 and 37, Takeuchi discloses a semiconductor device (fig. 3) comprising:

asubstrate 24 having first and second opposing surfaces, the substrate having a plurality of signal lines and power lines and an integrated chip 16 mounted on the substrate.

Takeuchi fails to disclose the semiconductor device comprising the signal lines disposed between a pair of the plurality of first power lines and the plurality of first power lines disposed between a pair of the second power lines.

Tsubosaki et al. discloses a semiconductor device (fig. 3) comprising:

a plurality of signal lines 7-8 and 10-11 (column 5, lines 30-37), a plurality of first power lines 6 and 12 coupleable to a first power source, and a plurality of second power lines 1 and 14, all on the same surface, at least one of the plurality of signal lines disposed between a pair of the plurality of first power lines 6 and 12, and the signal lines

between the pair of the plurality of first power lines and the pair of the plurality of first power lines disposed between a pair of the second power lines 1 and 14. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Takeuchi to provide a thin, inexpensive, high performance, as shown by Tsubosaki et al.

- Regarding claims 31 and 38, Takeuchi discloses the signal lines 10 are of a first width, the first power lines 12 are of a second width different from the first, and the second power lines 14 are of a third width different from the first and the second widths (fig. 3, column 6, lines 34-40).
- Regarding claims 32 and 39, Takeuchi discloses the third width is wider than the second width, and the second width is wider than the first width (fig. 3, column 8, lines 5-7).
- Regarding claim 33, Takeuchi discloses a ground plane 28 on the first surface of the substrate.
- Regarding claim 34, Takeuchi discloses a semiconductor device (fig. 3) comprising:

a substrate 24 having first and second opposing surfaces, the substrate having a plurality of groups of lines, the plurality of groups of lines including groups of lines of at least three different widths disposed on the second surface of the substrate, the signal lines 10 with first width, the first power lines 12 with second width and the third power lines with third width and an IC chip 16 mounted on the substrate and coupled to at least some of the lines.

Takeuchi fails to disclose the semiconductor device comprising the signal lines disposed between a pair of the plurality of first power lines and the plurality of first power lines disposed between a pair of the second power lines.

Tsubosaki et al. discloses a semiconductor device (fig. 3) comprising:

a plurality of signal lines 7-8 and 10-11 (column 5, lines 30-37), a plurality of first power lines 6 and 12 coupleable to a first power source, and a plurality of second power lines 1 and 14, all on the same surface, at least one of the plurality of signal lines disposed between a pair of the plurality of first power lines 6 and 12, and the signal lines between the pair of the plurality of first power lines and the pair of the plurality of first power lines disposed between a pair of the second power lines 1 and 14. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Takeuchi to provide a thin, inexpensive, high performance, as shown by Tsubosaki et al.

- Regarding claim 35, Takeuchi discloses the lines of the first width are signal lines 10, the lines of the second width are power lines 12 coupled to a first voltage potential, and the lines of the third width are power lines coupled to a second voltage potential.
- Regarding claim 36, Takeuchi discloses a ground plane 28 on the first surface of the substrate.

3. Claims 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Washida et al. (U.S. Pat. 5877548) in view of Takeuchi (U.S. Pat. 5497030).

Washida et al. fail to disclose the lines of the first width are signal lines, the lines of the second width are power lines coupled to a first voltage potential, and the lines of the third width are power lines coupled to a second voltage potential.

Takeuchi discloses a semiconductor device (fig. 3) comprising: the lines of the first width are signal lines 10, the lines of the second width are power lines 12 coupled to a first voltage potential, and the lines of the third width are power lines 14 coupled to a second voltage potential. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Washida et al. to have a satisfactory performance in the high frequency semiconductor device, as shown by Takeuchi.

- Regarding claim 36, Takeuchi discloses a ground plane 28 on the first surface of the substrate (fig. 3, column 4, line 51).

***Claims Allowed***

Claims 1-22 are allowed (see the previous examiner's statement of reasons for allowance).

***Response to Arguments***

Applicant's arguments filed 12/2/03 have been fully considered but they are not persuasive.

Applicant argues that the provisional filing date of the subject application is prior to that of Kalidas et al.

The examiner respectfully disagrees.

The provisional filing date of Kalidas et al. is prior to the provisional filing date of the subject application. Therefore, Kalidas et al. is available as a reference in this application.

Applicant argues that Stearns et al., Nemoto et al. and Cuvilliers et al. fail to disclose the currently amended claimed invention.

Stearns et al., Nemoto et al. and Cuvilliers et al. have been removed from the rejection. Therefore, see the new ground of the rejection above.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

DLN
March 5, 2004